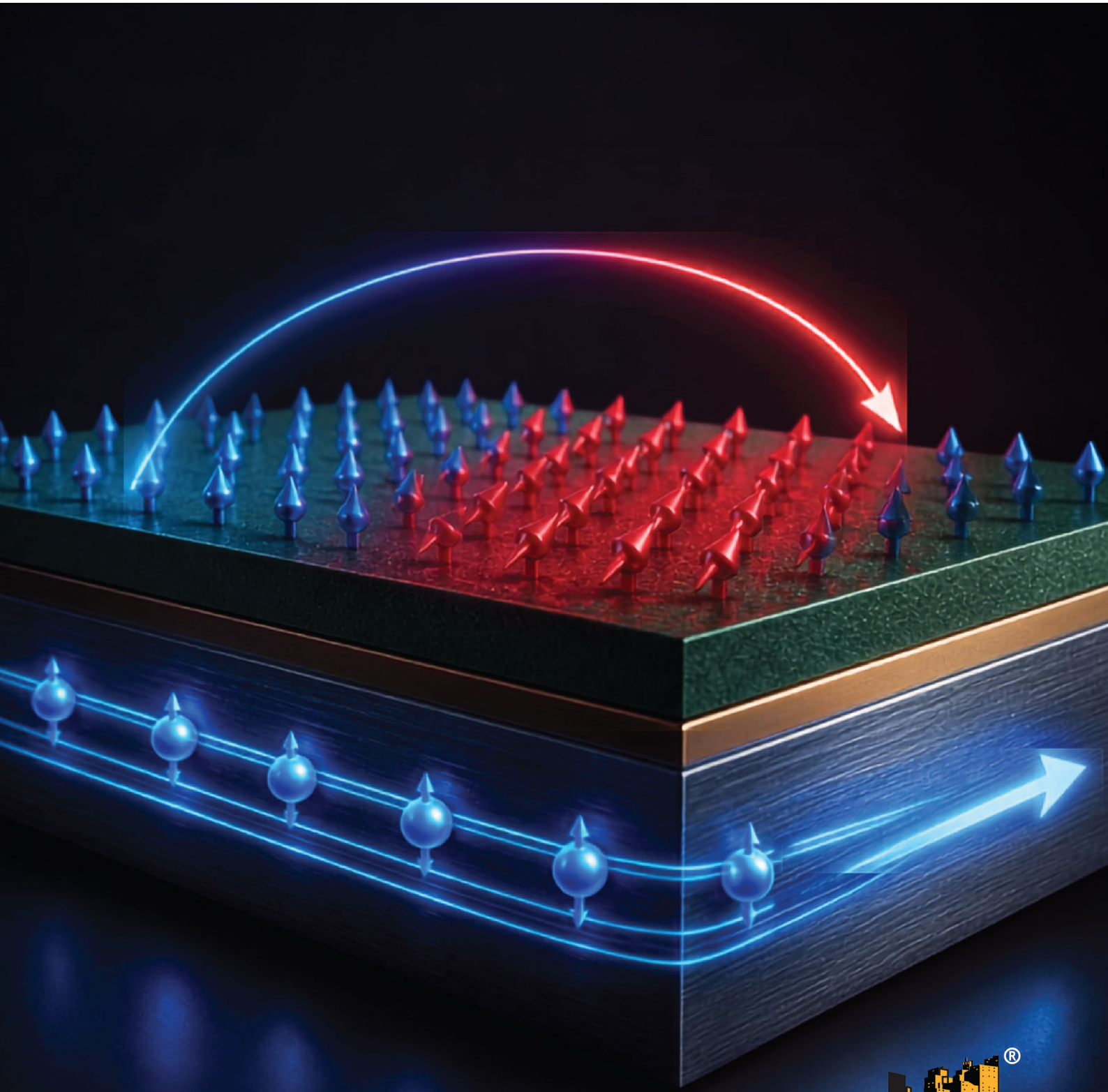
TECH SCAN

SPINTRONIC MEMORY TECHNOLOGIES



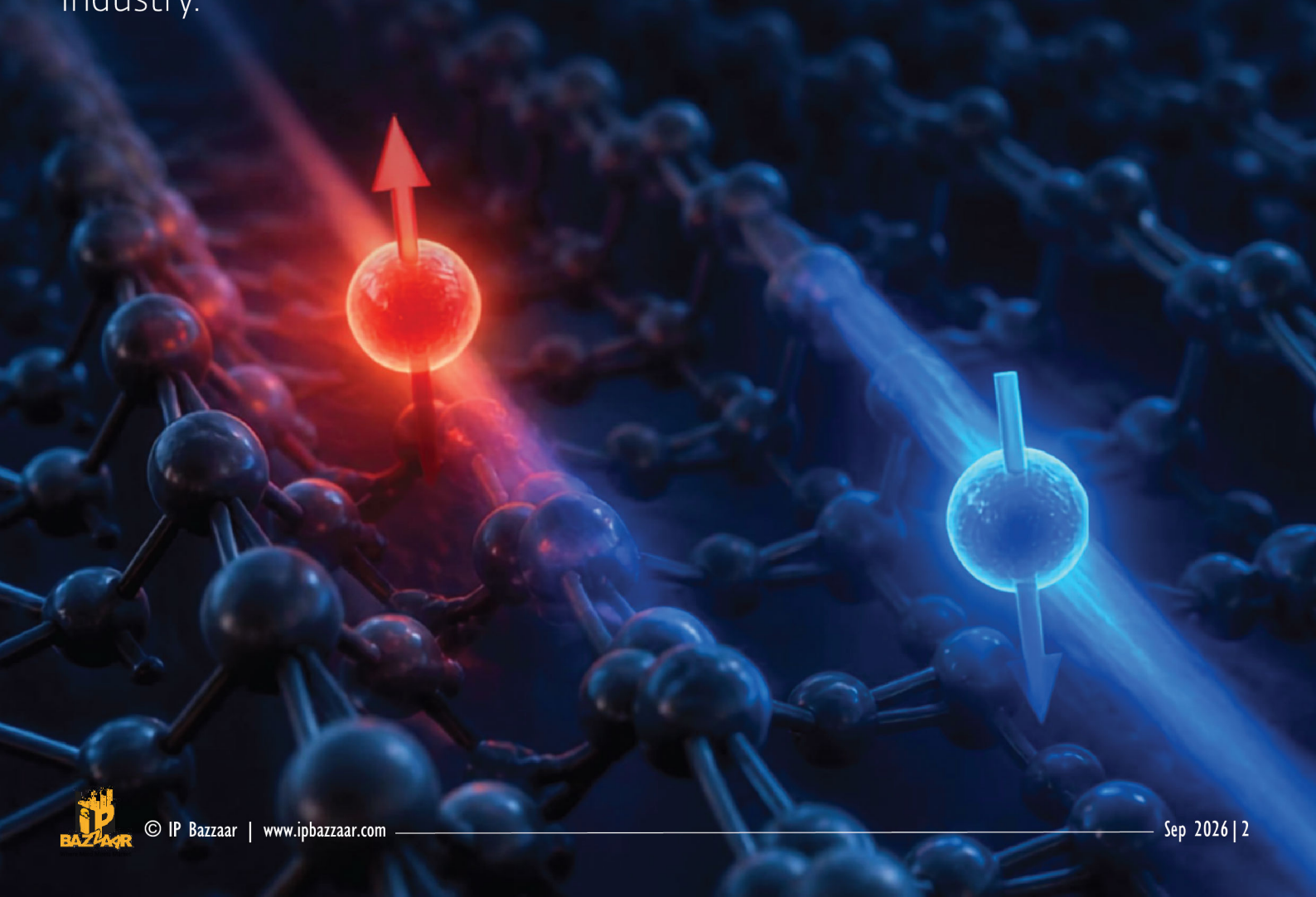
BAZAAR®

WHERE MIND MEETS MARKET

Spintronic memory technologies are emerging as a key advancement in semiconductor engineering. They offer an alternative to conventional charge-based memory systems by using electron spin for data storage. This approach supports energy-efficient operation, fast performance, and long-term data retention, making it suitable for applications such as artificial intelligence, data centres, edge computing, and automotive systems.

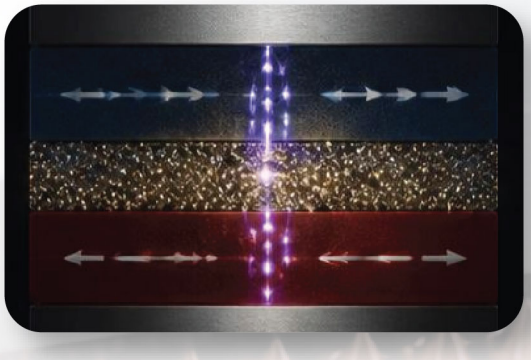
Unlike SRAM, DRAM, and flash memory, spintronic memory does not rely on continuous charge storage or refresh cycles. Instead, it uses magnetic states to store information, enabling non-volatile operation with lower power consumption, faster switching, and higher endurance. This makes spintronic memory a strong candidate for future high-performance computing architectures.

Research and development in spintronic memory focus on magnetic tunnel junctions, spin-transfer torque (STT), and spin-orbit torque (SOT) mechanisms. Innovations aim to improve switching efficiency, thermal stability, scalability, and device reliability. Patents in this field protect advancements in materials, device structures, and fabrication processes, supporting continued progress and competitiveness in the semiconductor industry.



INNOVATION TIMELINE

Foundational Physics & Giant Magnetoresistance (GMR) Era



1960s (IBM Spin Control Concept)
Leo Esaki proved spin-dependent transport.

1980s (Advanced Epitaxy Development)
Labs engineered multi-layer magnetic thin films.

1988 (Discovery of GMR)
Fert and Grünberg discovered GMR.

1995 (Room-Temperature TMR) Moodera demonstrated room-temperature MTJ tunneling.

1996 (Theoretical Framework of STT)
Slonczewski and Berger calculated STT.

2003 (IEEE Spintronics Launch)
IEEE consolidated foundational hardware methodologies.

2006 (Freescale's Standalone MRAM)
Freescale commercialized standalone Toggle-MRAM chips.

2007 (Nobel Prize Validation)
GMR discovery won Nobel Prize.

2011 (Toggle-MRAM Deployment)
Industries deployed early aerospace Toggle-MRAM.

2014 (Perpendicular MTJ Breakthrough)
Everspin shipped vertical pMTJ architecture.

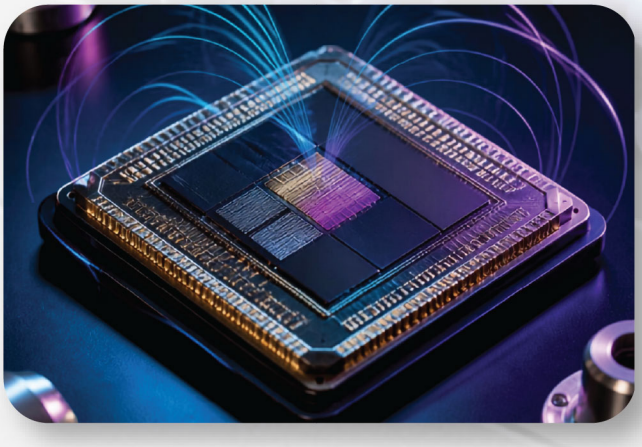
2019 (Foundry Integration of STT-MRAM)
Foundries embedded STT-MRAM onto wafers.

2021 (Multi-Level Cell Milestones)
Engineers validated multi-bit MTJ storage.

2023 (FinFET Node Spintronics)
Foundries integrated MRAM into FinFETs.

2024 (SOT-MRAM Advanced Pilot Lines)
IMEC deployed sub-nanosecond SOT lines.

2026 (VCMA & Skyrmion Convergers)
Designers paired low power VCMA with skyrmions.



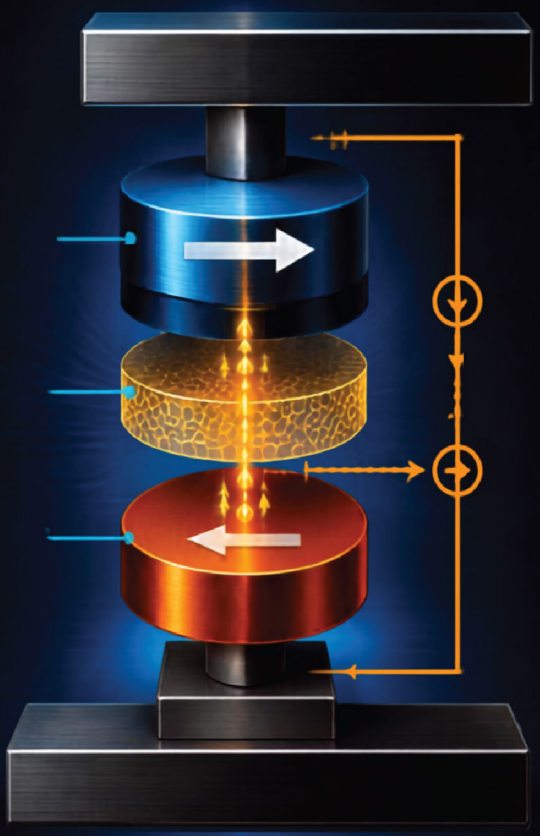
PATENTABLE COMPONENTS

1. Material Science & Core Layer Stacks (The Physical MTJ) This domain targets advanced material compositions and thin-film physics to maximize the reading signal (TMR ratio) and lower power thresholds.

- Perpendicular Free-Layer (pFL) Caps / Layers
- Crystalline Magnesium Oxide (MgO) Tunnel Barriers
- Synthetic Antiferromagnet (SAF) Reference Blocks / Layers
- Heavy Metal Spin-Hall Micro-tracks / SOT Underlayers
- Topological Insulator Interfaces
- Altermagnetic Spin-Splitter Liners
- 2D Van der Waals (vdW) Ferromagnetic Sheets

2. Electrical Routing, Ports & Switching Mechanisms
This domain covers the hardware pathways used to inject, manipulate, and flip spin vectors within the memory cells.

- STT Injection Ports
- SOT Decoupled Tracks
- VCMA Voltage Gates
- Asymmetric Field-Free Geometrical Wedges
- Domain-Wall Plasticity Channels



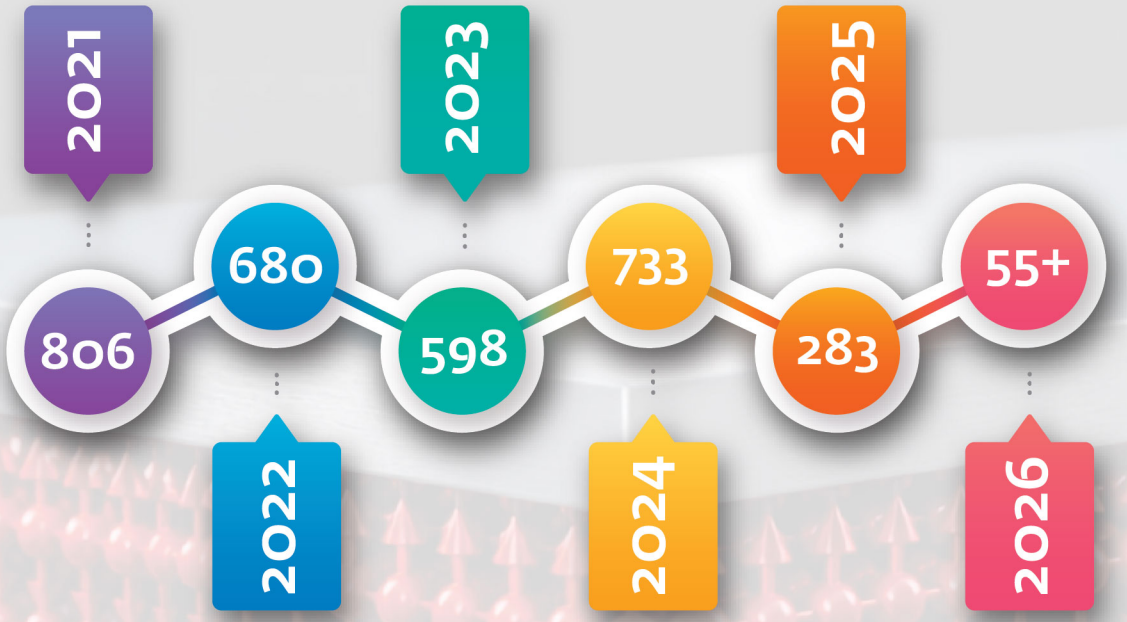
3. Fabrication Methods & Material Processing (Manufacturing) This domain encompasses the foundry processes used to etch, insulate, and stack magnetic layers onto silicon without causing structural or crystal edge damage.

- Passivation Encapsulation Liners
- Ion Beam Etching (IBE) Sacrificial Masks / Stop-Layers
- Bottom & Top Electrode Plugs
- Monolithic 3D BEOL Via Plugs

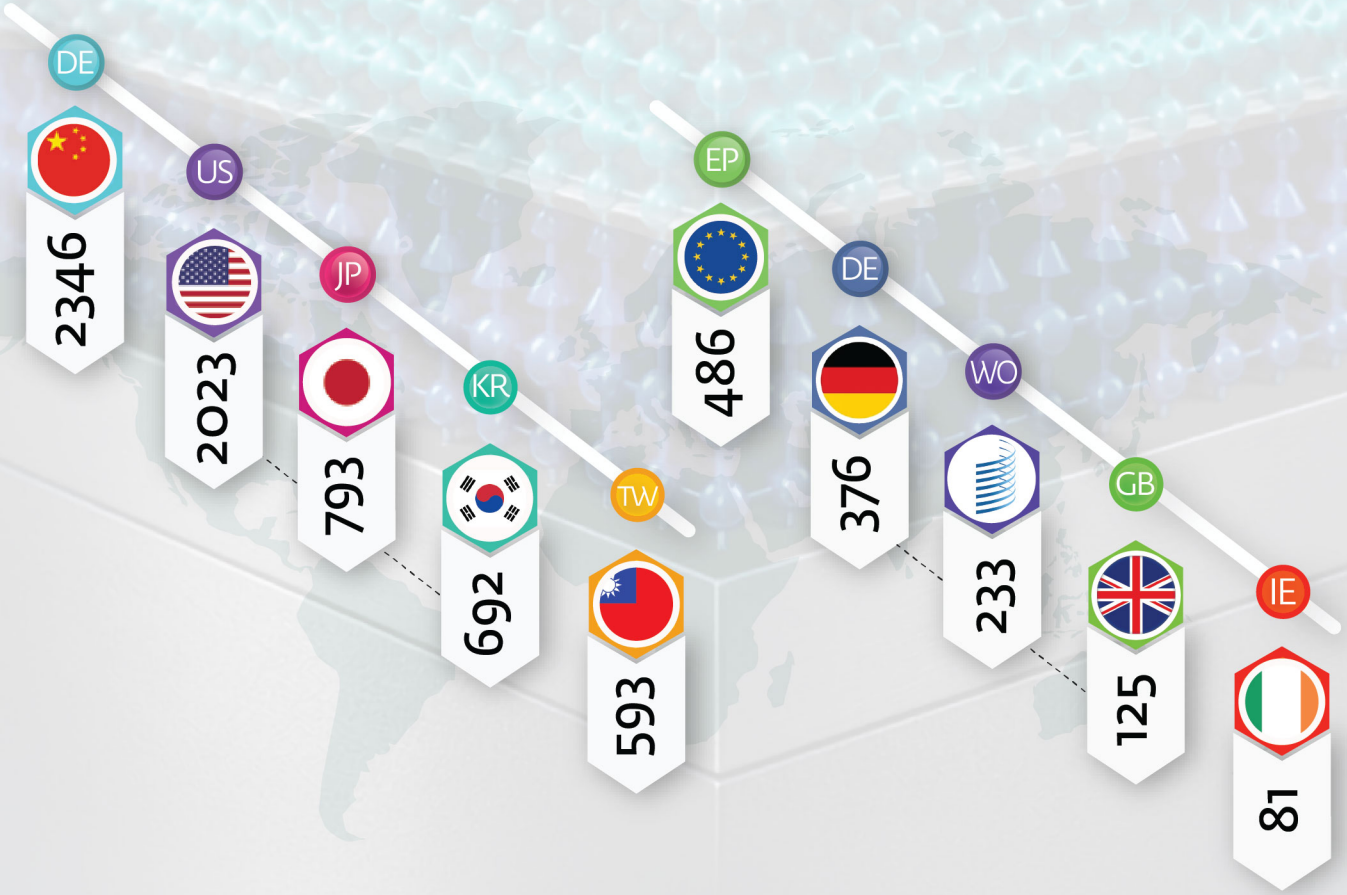
4. Memory Array Circuits & Computing Modules (System Layouts)
This domain focuses on the peripheral CMOS circuitry that reads, writes, and processes data around the magnetic core.

- 1T-1MTJ Shared-Source Bit-Cells
- High-Margin Dynamic Sense Amplifiers
- Low-Overhead High-Endurance Write Drivers
- Compute-In-Memory (CIM) Spintronic Fabrics
- Stochastic True-Random-Number Generators (TRNG)

PATENT STATISTICS



PATENT LANDSCAPE



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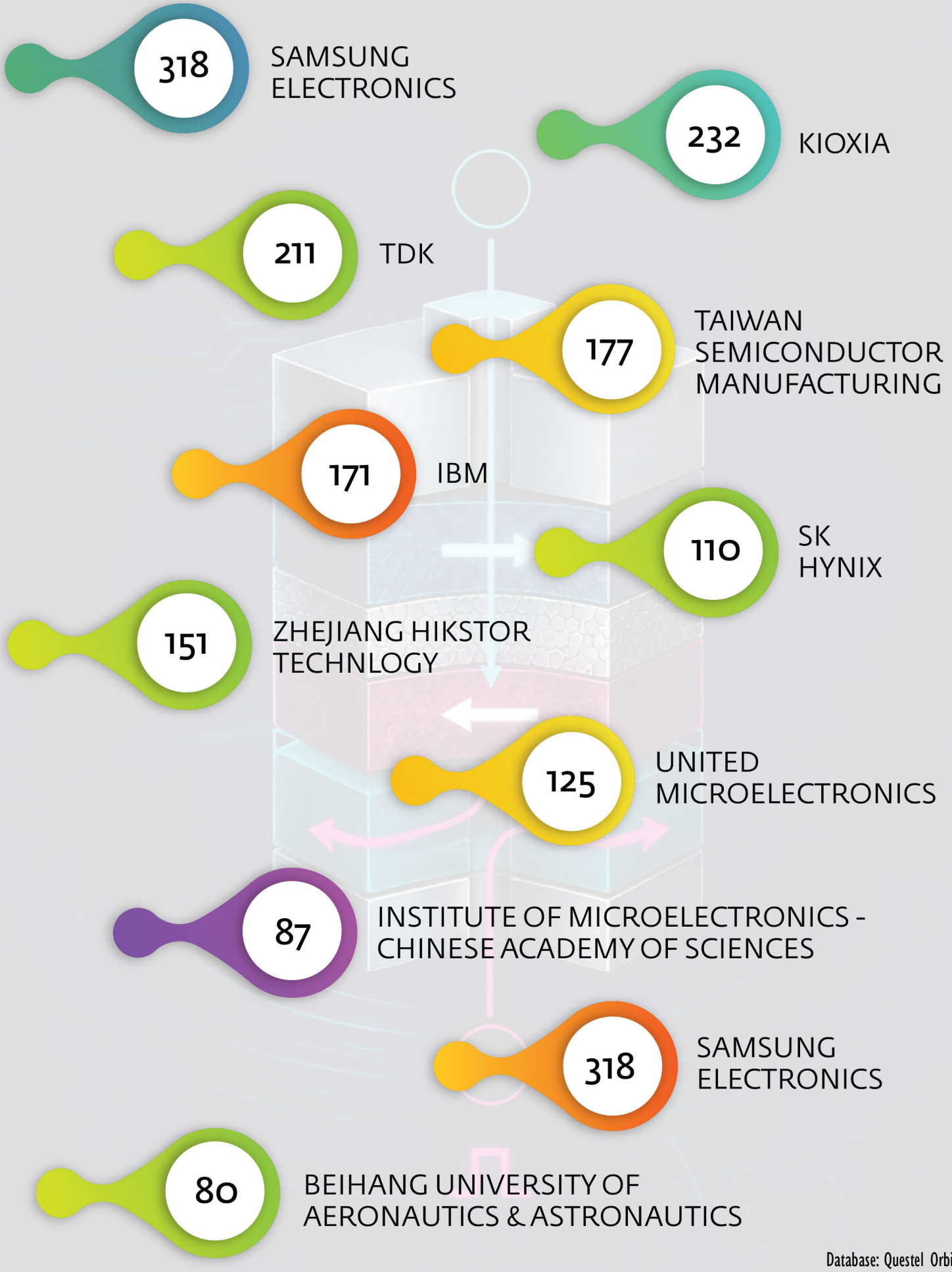
TOP APPLICANTS



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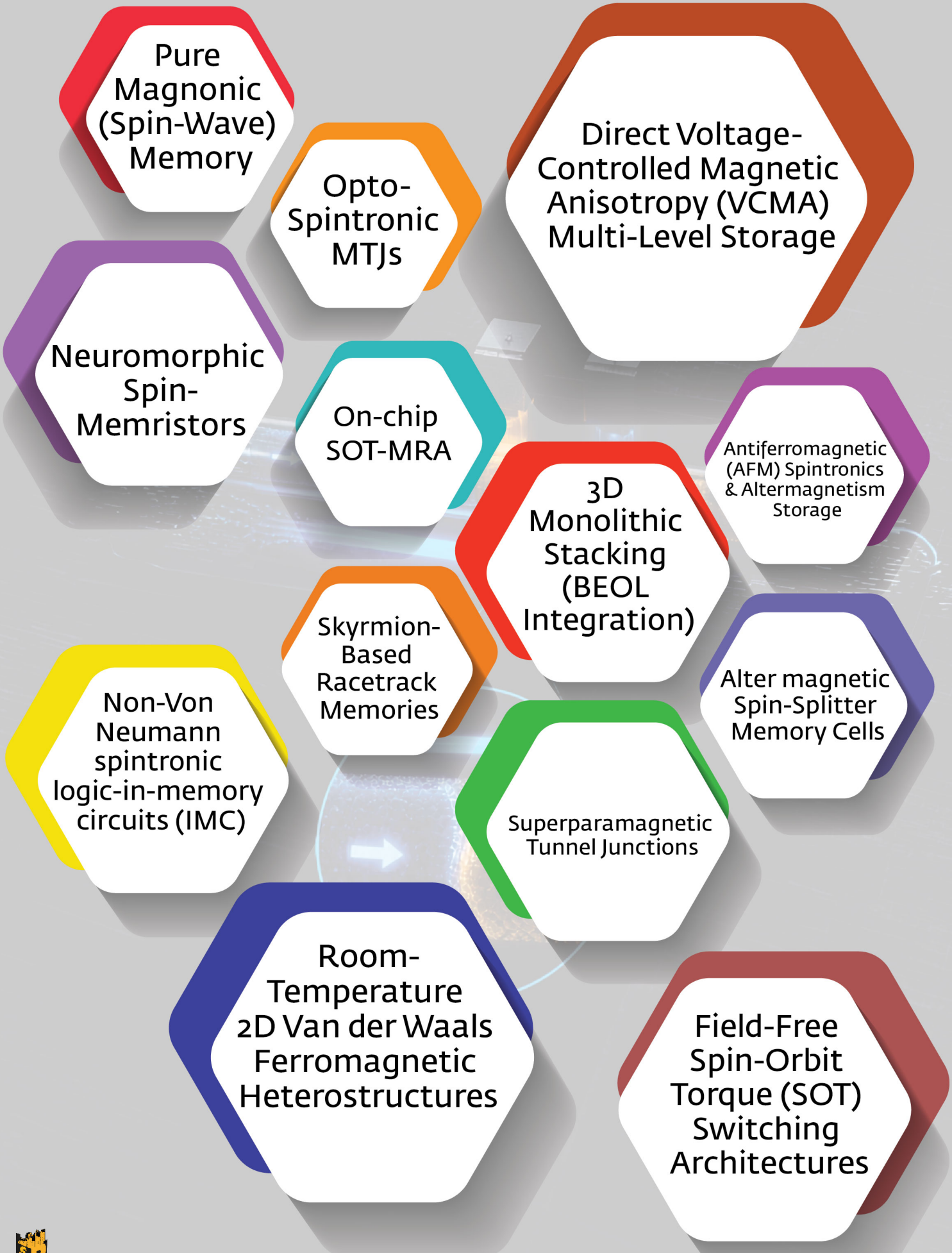
Data Range: 01/01/2021 - 10/07/2026

NOTABLE INNOVATIONS

Patent Application	Priority date	Title	Assignee
DE1126485 B	29.03.1962	Semiconductor device with magnetoresistance and method of manufacturing the same	Siemens
FR91063 E	04.05.1968	Method of manufacturing magnetic memory device	PHILIPS
US6278631	03.08.1998	Magnetic random access memory array divided into a plurality of memory banks	EVERSPIN FREESCALE SEMICONDUCTOR
US6479848	03.02.2000	Magnetic random access memory with write and read circuits using magnetic tunnel junction (MTJ) devices	SAMSUNG ELECTRONICS
US8120947	22.05.2007	Spin torque transfer MRAM device	TAIWAN SEMI-CONDUCTOR MANUFACTURING
US8750013	04.01.2013	Racetrack memory with low-power write	IBM
US20190013353	07.03.2016	Approaches for integrating stt-mram memory arrays into a logic processor and the resulting structures	INTEL
JP7095490	27.08.2018	Spin-orbit torque-type magnetized rotary element, spin-orbit torque-type magneto-resistive effect device, and magnetic memory	TDK
WO2026/061604	17.09.2024	A 3d vertical magnetic memory device	IMEC - INTERUNIVERSITAIR MICRO ELECTRONICA CENTRUM
US20250285697A1	03-06-2025	Spintronic adaptive approximate memory (SAAM) architectures for neural network workloads	IBM

WHITESPACES



If you would like to learn more about any of these areas or have specific questions, we're here to provide further information and insights. Our team is dedicated to driving progress and staying at the forefront of Spintronic Memory Technologies.

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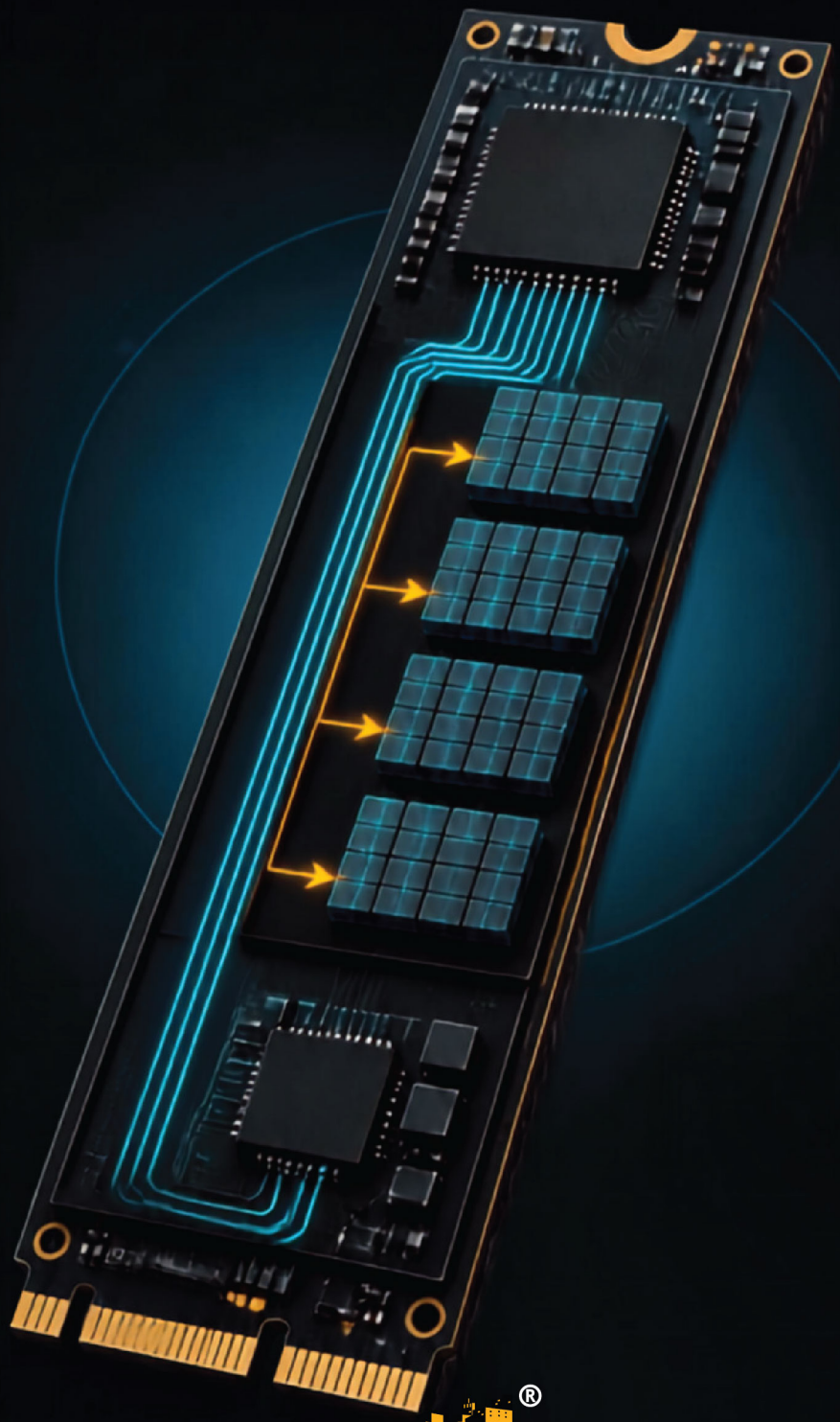

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